Display Technology Letters

Driving Scheme Using Bootstrapping Method for Blue-Phase LCDs

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***Abstract*—We present a new pixel circuit on glass using hydrogenated amorphous silicon (a-Si:H) for driving polymer-stabilized blue-phase liquid crystal displays (BPLCDs). Different from conventional nematics, BPLC demands a large dielectric anisotropy in order to lower the operation voltage. As a result, the pixel's capacitance is increased by $\sim 10\times$, which seriously limits the charging capability and optical efficiency. Simulation results show that the average error rate of storage voltage in pixel circuit is below 5.14% for 180 Hz operating frequency.**

***Index Terms*—Blue-phase liquid crystal (BPLC), driving circuit, hydrogenated amorphous silicon (a-Si:H).**

I. Introduction

POLYMER-STABILIZED blue-phase liquid crystal (BPLC) is emerging as next-generation display technology due to its submillisecond response time, no need for alignment layer, and optically isotropic dark state [1], [2]. Especially, fast response time [3], [4] enables color sequential display with RGB LEDs so that the optical efficiency and resolution density are all tripled. In-plane switching (IPS) electrodes [5], [6] are widely used in BP LCDs because the backlight can be set at normal incidence so that high contrast and wide view can be achieved easily. However, two shortcomings are found: the required operating voltage is fairly high (~50 V) and hysteresis is large (~6%) due to the strong electric fields at the edge of electrodes [5]. Several approaches, such as protrusion electrodes [8]–[10], wall-shaped electrodes [11], and corrugated electrodes [12], have been proposed to lower the driving voltage and hysteresis. The major tradeoff is the increased device fabrication complexity. To simply fabrication process, vertical field switching (VFS) mode has been proposed [13], which greatly reduces the operating voltage and suppresses the hysteresis. The remaining challenge for the VFS mode is to achieve wide viewing angle [14], [15].

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Unlike conventional nematic LCs, BPLC demands an unusually large dielectric anisotropy ($\Delta\varepsilon$) to achieve low voltage operation. As a matter of fact, BPLCs with $\Delta\varepsilon > 100$ have been developed [16], [17]. In addition to high viscosity, these huge $\Delta\varepsilon$ BPLCs produce a large capacitance (Clc), leading to insufficient charging capability in conventional pixel circuit, i.e. the voltage applied to the LC capacitor cannot reach the desired value within the designated charging time. As a result, the optical efficiency is sacrificed. Especially, in color sequential displays, the driving frequency is tripled, so that the charging problem becomes more severe.

In the paper, we propose a new circuit for driving the blue-phase LCDs. Compared to conventional pixel circuit, the newly proposed pixel driving circuit employs an additional signal to keep the aperture ratio while improving the insufficient charging capability of pixel circuit.

II. Circuit Schematic and Operation

Fig. 1 shows the voltage-dependent transmittance (VT) curves for IPS and VFS cells. The electrode width/gap/cell gap for the IPS cell is 10/10/7.5 μm. The cell gap for the VFS cell is 5.7 μm. The material preparation process is described as follows: The BPLC mixture employed is JNC JC-BP01M [15]. We filled the IPS and VFS cells by capillary flow. The phase transition temperature was BP 42.4 °C N^* during the cooling process and N^* 44.5 °C BP during the heating process, where N^* stands for chiral nematic phase and BP for blue phase. UV exposure was performed at 44 °C with an intensity of 2 mW/cm^2 for 30 min. After UV curing, we measured the VT curves at room temperature using a He–Ne laser ($\lambda = 633$ nm). The measurement method has been reported in [13]. For VFS cell, the incident angle is $\theta = 70°$.

From Fig. 1, the VFS cell (black line) has a much lower on-state voltage (16 $V_{\rm rms}$) than IPS (red line; 54 $V_{\rm rms}$). To further lower the driving voltage to ~10 V, we purposely reduce the cell gap to 3 μm, increase the incident angle to 75° and change the central wavelength to 550 nm. The dashed lines show the simulated curve and its capacitance can be calculated easily from following equation:

$$Clc = \frac{\varepsilon \times \varepsilon_0}{d} \times A \tag{1}$$

where ε, d, and A denote the relative dielectric constant, BPLC cell gap, and total area of the BPLC cell, respectively, and ε_0 is 8.854×10^{-12} F/m. For the BPLC used, $\varepsilon \approx 72$ at room temperature and $V = 0$. For a pixel size of 120 μm × 360 μm, the calculated LC capacitance is ~9 pF, which is about 10× larger than that of a traditional nematic LC, leading to an insufficient charging capability in pixel circuit. From (1), one way to

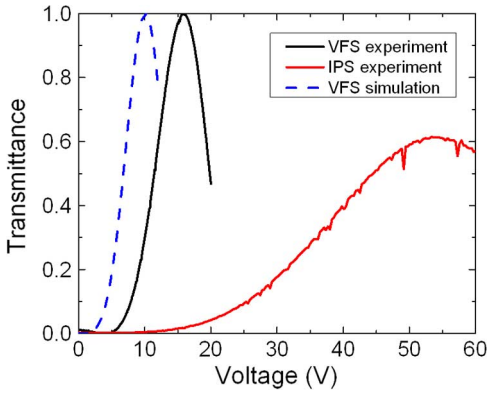

Fig. 1. Measured VT curves for IPS (red) and VFS (black) cells at room temperature (T $\sim$ 23 °C). VFS cell: cell gap of $d = 5.7$ μm, incident angle of $\theta = 70°$ and $\lambda = 633$ nm. Dashed blue lines represent the simulated curve for a VFS cell with $d = 3$ μm, $\theta = 75°$ and $\lambda = 550$ nm

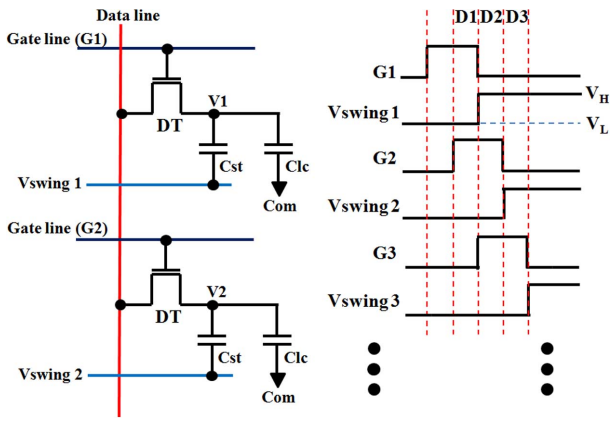

Fig. 2. Proposed driving scheme and its timing diagram.

reduce Clc is to employ a smaller dielectric anisotropy BPLC and a thicker cell gap. However, the former would lead to a smaller Kerr constant and the latter to a weaker electric field, which in turn decreases the induced birefringence. According to [14], larger Kerr constant and thinner cell gap are favorable for reducing the operation voltage. With these constraints, we need to develop new driving scheme for overcoming the large capacitance problem of BPLC.

Fig. 2 shows the proposed driving scheme and its timing diagram for BP-LCDs. Here, a driving thin-film transistor (DT) is controlled by the gate line while the data line provides a data voltage to the pixel circuit, where Cst represents the storage capacitor for memorizing the data voltage, and Clc represents the effective capacitor of BPLC. Moreover, based on an additional control signal ($V_{\rm swing}$) two constant voltages ($V_{\rm H}$ and $V_{\rm L}$) are supplied by the capacitor coupling of Cst.

Circuit operations can be divided into following two stages:

A) *First stage:* when the gate line (G2) goes to a high voltage while G1 is maintained at a high voltage, the data voltage (D1) is transmitted to V1 node of the current pixel circuit and can pre-charge V2 node of the next pixel circuit to extend the charging time. Next, G1 is changed from high to low voltage and the new data voltage (D2) is supplied to V2 node of pixel circuit.

B) *Second stage:* when the gate line (G2) goes to a low voltage, the additional signal ($V_{\rm swing}$ 2) is changed from $V_{\rm L}$ to $V_{\rm H}$ to couple a constant voltage (ΔV) to the V2 node. Therefore, the stored voltage of V2 node can be expressed as follows:

$$V2 = D2 + (V_H - V_L)\frac{Cst}{Cst + Clc + Ceq} \qquad (2)$$

where Ceq denotes the parasitic capacitance of DT.

Compared to the conventional pixel circuit, the new driving scheme via capacitor coupling method can reduce the data voltage swing, enhance the driving capability, and reduce power consumption of the panel.

III. Results and Discussion

The stored voltage in pixel circuits is simulated using software HSPICE. The characteristics of TFT are then matched using the Rensselaer Polytechnic Institute (RPI) model. Therefore, simulated model parameters are obtained by measuring a-Si:H TFT and RPI (level = 61) for this model. Although the LTPS and a-IGZO devices are more effective than a-Si:H device in driving circuits, to ensure applicability to large panels and to benefit from a mature manufacturing process, a-Si:H was chosen herein. Therefore, the mobility, width, length, Cgd, and Cgs of a-Si:H TFT (DT) were about 0.2 $\rm cm^2/V \cdot s$, 96 μm, 5.5 μm, 3 fF, and 9 fF, respectively. Voltage swings of gate line and data line are -13 V to 27 V and -10 V to 10 V, respectively. Cst and cell gap are 1 pF and 3 μm, respectively. Notably, Clc is set to 9 pF for a 120 μm $\times$ 360 μm pixel size. Also, the value of $V_{\rm swing}$ depends on the Cst and Clc. Therefore, in this case, to obtain the 5 V coupling voltage, the $V_{\rm swing}$ is designed from 0 V to 51.1 V. The $V_{\rm swing}$ of the proposed circuit is set at 51.1 V, and it changes only once per frame (16.7 ms). Also, the proposed pixel circuit with capacitor coupling effectively reduces the data voltage swing and can be modified according to the actual device conditions, such as using a low voltage and low capacitance BPLC in small pixels. Additionally, while assuming that a FHD (1920$\times$1080) display with 60 Hz, 120 Hz, and 180 Hz refreshing frequencies is used, the gate pulse widths of each RGB subpixel are 30 μs, 15 μs, and 10 μs with a pre-charge method.

The dashed blue lines in Fig. 1 represent the VFS BP-LCD we intend to use. Its peak voltage is 10 V. Fig. 3(a) shows the dynamic response of the stored voltages. While the data voltage is 10 V, the maximum storage voltages of conventional pixel circuit in 60 and 120 Hz driving frequencies are 9.95 and 9.37 V, respectively. Although the stored voltage under 60 Hz frame rate is very close to the data voltage, the voltage error rate of a conventional pixel circuit with a high frequency (120 Hz) is 6.3%. Compared to a conventional pixel circuit in Fig. 3(b), the data voltage is decreased to 5 V and combined with a capacitor coupling method. When the driving frequencies are 60 Hz and 120 Hz, the stored voltages of the proposed pixel circuit are 10 and 9.84 V, respectively. Moreover, the voltage error of proposed pixel circuit is reduced to 1.6%. Even the stored voltages associated with different frequencies are simulated for up to the period of one frame (16.7 ms), the stored voltage decays from 10 to 9.87 V for the 60 Hz driving frequency. As the driving frequency increases to 120 Hz, it decays from 9.84 to 9.72 V.

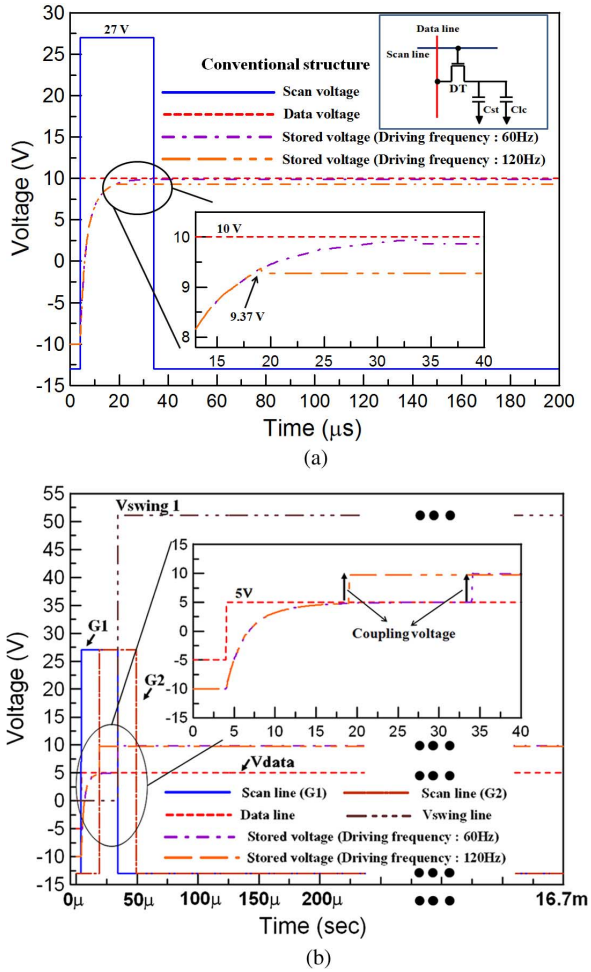

Fig. 3. Stored voltages in Cst with a data voltage. (a) conventional structure and (b) proposed structure.

Therefore, although the charges of the pixels naturally decay, the stored voltages also decrease slightly.

Fig. 4 depicts the simulated VT curves of conventional circuit and proposed circuit. Compared to the initial state, the VT curves of conventional circuit and proposed circuit correlate well with each other for the 60 Hz operating frequency. However, the deviation increases gradually as the operation frequency increases from 60 Hz to 120 Hz and 180 Hz. Simulation results indicate that the transmittance of the conventional circuit is decayed to 0.863 while that of the proposed circuit is decreased only to 0.976 when the applied voltage of conventional circuit and proposed circuit are 10.08 V and 5.08 V, respectively. According to Fig. 5, the average stored voltage error rate of conventional circuit is ∼13.5% and ∼5.14% for the proposed circuit at 180 Hz. Next, we simulated the driving frequency for 240 Hz. The average stored voltage error rate of the conventional pixel circuit at 240 Hz is increased to ∼25.05% and that of the proposed pixel circuit is ∼11.13%. Although the error rate achieved using the proposed pixel circuit is increased at 240 Hz, it is 55.6% smaller than that of the conventional pixel circuit. We believe this error rate can be further reduced. Therefore, simulated results demonstrate that the proposed pixel circuit can improve the insufficient charging

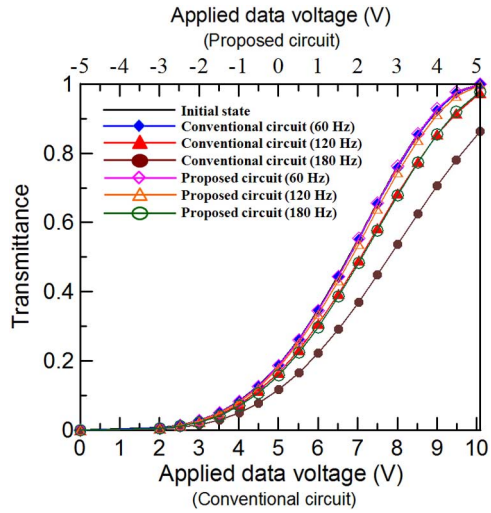

Fig. 4. Simulated VT curves of initial state, conventional circuit, and proposed circuit.

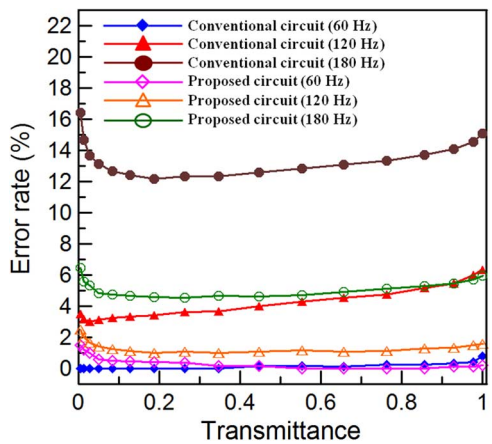

Fig. 5. Simulated stored voltage error rates of conventional circuit and proposed circuit.

capability of conventional pixel circuit and stably store the data voltage to drive the BPLC effectively.

IV. Conclusion

This work presents a new driving scheme using a-Si:H TFT for blue-phase LCDs with the VFS mode. The proposed pixel circuit is superior to the conventional pixel circuit in performance with respect to stored voltage while operating at high frequencies. Simulation results indicate that the average stored voltage error rate at 180 Hz operation is below 5.14% which is still acceptable for color sequential display applications.

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