Transflective LCDs With Two TFTs and Single Data Line

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***Abstract*—A simplified single-cell-gap transflective liquid crystal display with two thin-film-transistors and only one data line is proposed. The simulated voltage-dependent transmittance (VT) and reflectance (VR) curves overlap reasonably well, which enables a single gamma curve driving. The need of only one data line improves the aperture ratio, reduces the fabrication cost, and stabilizes the manufacturing process.**

***Index Terms*—Single gamma curve, thin-film transistors (TFTs), transflective liquid crystal display (LCDs).**

I. Introduction

SIGNIFICANT advances in portable electronics such as cellular phones and personal digital assistants [1]–[8] have led to stringent requirements for panels with a wide viewing angle, good sunlight readability, lightweight, and low power consumption. Given the above requirements, sunlight readable transflective liquid crystal display (TR-LCD) is highly desirable for mobile display applications. Each pixel of a TR-LCD is normally divided into transmissive (T) and reflective (R) regions. The T region transmits a backlight while R region makes use of the ambient light. In the T region, backlight passes through the LC layer once, while in the R region, the ambient light traverses the LC twice. Dual-cell-gap [8] and single-cell-gap [1]–[4] approaches have been developed to compensate for the optical path difference in these two regions. Dual-cell-gap approach offers a good match between voltage-dependent transmittance (VT) and reflectance (VR) curves. Thus, although a single gamma curve can be used, its fabrication process is more complicated [2]. On the other hand, single-cell-gap TR-LCD has a simpler structure, but its driving scheme is more complicated.

Sheu *et al.* [1] designed a pixel circuit with double gamma method (DGM) to achieve matched VT and VR curves. However, each pixel requires an additional data line, subsequently reducing the aperture ratio. While attempting to avoid the complexity of the double gamma method, Kang *et al.* [2] developed a capacitance divided vertical-alignment (VA) LC cell with a single gamma method to drive the T- and R- modes simultaneously. However, an additional organic layer is still required in the fabrication. Additionally, the residual DC voltage on a floating electrode causes image sticking [9]. Moreover, Yang *et al.* [3] designed a pixel structure called the capacitor coupled reflective (CCR) mode for TR-LCDs. In this approach, reflective part is divided into two regions and different voltages are applied to each region to achieve a matched VT and VR curves. However, this mode also incurs image sticking. Ge *et al.* [4] developed a switchable transflective circuit with high image quality under different ambient environments. Nevertheless, this circuit requires an extra control signal line for selecting the operation mode, subsequently complicating the circuit operations.

This work presents a single-cell-gap TR-LCD with an improved pixel circuit design, consisting of two TFTs and only one data line to provide matched VT and VR curves. Use of a single data line improves the aperture ratio, reduces the fabrication cost, and stabilizes the manufacturing process.

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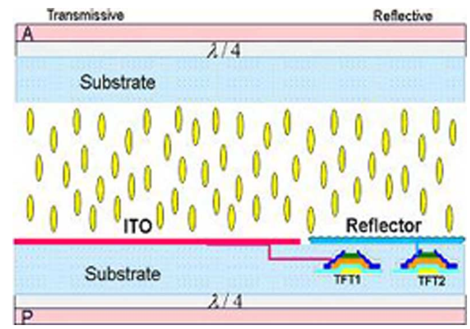

Fig. 1. Pixel structure of the single-cell-gap 2-TFT TR-LCD. Two TFTs are embedded under reflector. A and P represent crossed polarizers.

II. Circuit Schematic and Operation

Fig. 1 shows the pixel structure of the single-cell-gap VA-mode TR-LCD. The linear top polarizer and $\lambda/4$ plate form a circular polarizer in order to achieve high contrast ratio for the reflected mode [10]. Each pixel consists of T and R parts. In the R region, there is an embedded bumpy reflector to reflect the ambient light. Since the cell gaps for the two regions are the same, different voltages are required to drive the T and R regions in order to achieve the same phase retardation. Here, the 2-TFT approach is adopted as follows: TFT_1 is connected to the electrodes in the T region while TFT_2 provides the driving voltage to the R region. To improve the aperture ratio of the T region, these two TFTs are embedded under the bumpy reflector.

Fig. 2(a) depicts the proposed 2-TFT circuit and its timing diagram. Scan and data lines are used together to drive TFT_1 and TFT_2. $Cst1$ and $Cst2$ in the pixel circuit are storage capacitors used to memorize the data voltages V_A and V_B for the T and R regions, respectively. $Clct$ and $Clcr$ are the respective LC capacitors (49–154 fF) in T and R regions. Fig. 2(b) shows the equivalent model of the proposed circuit where Ceq_1 is the equivalent capacitance of $Cst1$ and $Clct$; Ceq_2 is the equivalent capacitance of $Cst2$ and $Clcr$; $r_{\rm on}$ is the channel resistance of a TFT when it is turned on and its value could be adjusted by varying the width and length of a TFT.

Circuit operations can be divided into the following two stages.

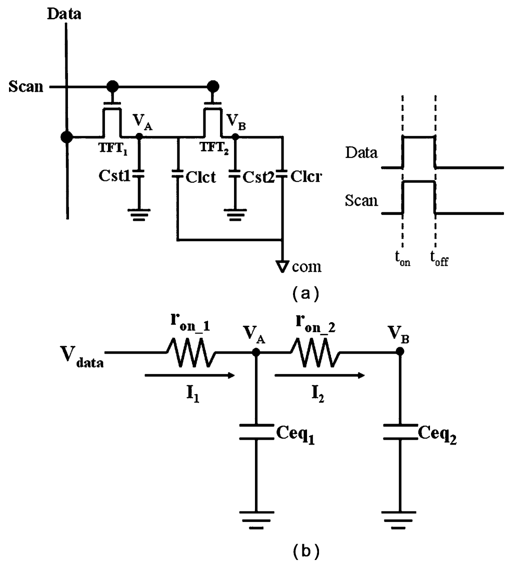

Fig. 2. Proposed circuit structure. (a) Proposed circuit and its timing diagram. (b) Equivalent circuit.

A. First Period

At time $t_{\rm on}$, when the scan line goes to a high voltage, TFT_1 and TFT_2, which operate in the triode region, are turned on and the charging process begins. During this period, V_A and V_B can be determined by the following equations:

$$V_{\rm data}-V_A = r_{\rm on\_1}\left(Ceq_1\frac{dV_A}{dt}+Ceq_2\frac{dV_B}{dt}\right) \quad (1)$$

$$\begin{aligned}V_{\rm data}-V_B &= r_{\rm on\_1}\left(Ceq_1\frac{dV_A}{dt}+Ceq_2\frac{dV_B}{dt}\right) + r_{\rm on\_2}\cdot Ceq_2\frac{dV_B}{dt}\\ &= r_{\rm on\_1}\cdot Ceq_1\frac{dV_A}{dt}+(r_{\rm on\_1}+r_{\rm on\_2})\cdot Ceq_2\frac{dV_B}{dt}\end{aligned} \quad (2)$$

Solving (1) and (2) leads to

$$\begin{aligned}V_A &= (r_{\rm on\_2}Ceq_2c_1\lambda_1+c_1)e^{\lambda_1 t}\\ &\quad + (r_{\rm on\_2}Ceq_2c_2\lambda_2+c_2)e^{\lambda_2 t}+V_{\rm data}\end{aligned} \quad (3)$$

$$V_B = c_1e^{\lambda_1 t}+c_2e^{\lambda_2 t}+V_{\rm data} \quad (4)$$

where c_1, c_2, λ_1, and λ_2 are constants determined by $r_{\rm on\_1}, r_{\rm on\_2}$, Ceq_1, $Ceq_2, V_{\rm data}$, and the initial voltages of V_A $(T_{\rm on})$ and $V_B(T_{\rm on})$. Therefore, V_A and V_B vary as the charging time passes by.

B. Second Period

At $\mathrm{T}_{\rm off}$, when the scan line goes to a low voltage, TFT_1 and TFT_2 are turned off and the charging process stops. Thus, the voltages stored in $Cst1$ and $Cst2$ are maintained at $V_A(t_{\rm off})$ and $V_B(t_{\rm off})$, respectively. The voltage difference between them is

$$\begin{aligned}\Delta V(t_{\rm off}) &= V_A(t_{\rm off})-V_B(t_{\rm off})\\ &= r_{\rm on\_2}\cdot Ceq_2\cdot c_1\lambda_1e^{\lambda_1 toff}\\ &\quad + r_{\rm on\_2}\cdot Ceq\cdot_2 c_2\lambda_2e^{\lambda_2 toff}\end{aligned} \quad (5)$$

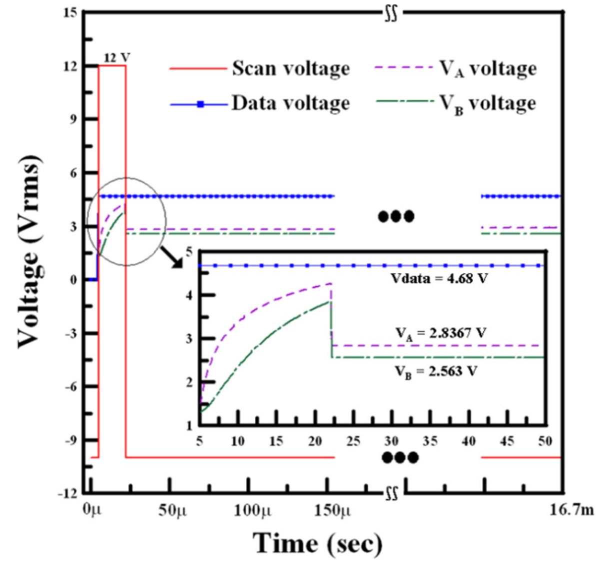

Fig. 3. Stored voltages in Cst1 and Cst2 with a data voltage of 4.68 $\mathrm{V_{rms}}$.

Therefore, properly adjusting $r_{\rm on}$, Ceq, and $V_{\rm data}$ allows us to distinguish between the stored voltages in T and R regions and match them with the required voltages.

III. Simulation Results

The stored voltages in $Cst1$ and $Cst2$ are simulated using software HSPICE. Also, the characteristics of the TFTs are matched using the Rensselaer Polytechnic Institute (RPI) model. Therefore, simulated model parameters are obtained by measuring a-Si:H TFT and RPI $(\text{level} = 61)$ for this model. The width, length, Cgd, and Cgs of TFT_1 are 16 μm, 5.5 μm, 496 fF, and 1.434 pF, respectively, while those of TFT_2 are 12.5 μm, 7.5 μm, 528.4 fF, and 1.527 pF, respectively. Voltage swing of the scan line ranges from -10 V to 12 V; $Cst1$, $Cst2$, and cell gap are 0.222 pF, 0.163 pF, and 4 μm, respectively. While assuming a QVGA (240*320) display is used and refreshing frequency is 60 Hz, the gate pulse of each R, G, B subpixel of the tri-gate structure [11] is about 17 μs.

Fig. 3 shows the dynamic response of storage voltages V_A and V_B. The data line is always kept at 4.68 $\mathrm{V_{rms}}$. At 5 μs, the scan line is turned on, and the charging process begins. According to this figure, V_A and V_B increase at a different rate. At 22 μs, the scan voltage is dropped to $-hbox10$ V, while V_A and V_B are kept at 2.8367 $V_{\rm rms}$ and 2.563 $V_{\rm rms}$, respectively. These values are very close to the required voltages for T and R regions, which are 2.8311 $V_{\rm rms}$ and 2.5031 $V_{\rm rms}$, respectively, at this gray level. Meanwhile, an abrupt voltage drop is observed at $t_{\rm off}$. Referred to as clock feedthrough, this phenomenon is caused by the parasitic capacitors of TFTs. Since the magnitude of voltage reduction is small and can be estimated [12], by proper designing the input data voltages, $Cst1$, and $Cst2$, the clock feedthrough effect can be minimized and the required voltages of T-mode and R-mode can be stored properly in $Cst1$ and $Cst2$, respectively.

Fig. 4 compares the stored voltages (V_A and V_B.) with the targeted voltages at different gray levels. The T-mode of a TR-LCD plays the primary role and the R-mode is mainly used under bright ambient [5]. Therefore, optimize the T-mode is of priority concern, i.e., to match V_A with the targeted voltages

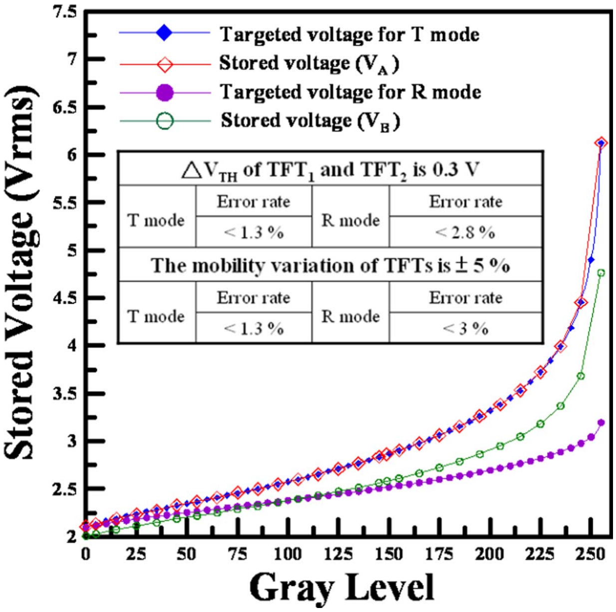

Fig. 4. Comparison of targeted and stored voltages at different gray levels for T-mode and R-mode.

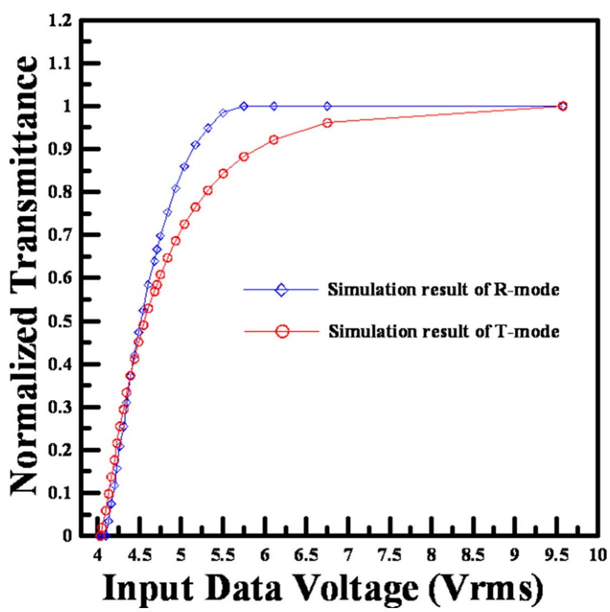

Fig. 5. Normalized VT and VR curves of the proposed new single-cell-gap 2-TFT TR-LCD.

in T-mode. Although the voltage V_B appears to diverge from the required voltage in R region at high gray levels, they match well at low and middle gray levels. Next, the variation of characteristics in TFTs is more closely examined. Simulation results indicate that the estimated maximum deviation of the stored voltage is less than 2.8% and 3% in T-mode and R-mode, while the $\triangle V_{TH}$ of TFT_1 and TFT_2 is 0.3 V and the mobility variation of TFTs is ±5%, respectively.

To evaluate the device performance to the first order, this work only calculates the transmittance and reflectance of the proposed TR-LCD at normal incidence. Hence, Fig. 5 depicts the normalized VT and VR curves of the new single-cell-gap, 2-TFT TR-LCD with only one data line. Notably, a situation in which the simulated stored voltage for R-mode exceeds than the highest required stored voltage, the corresponding input data voltages for R-mode are 100% normalized transmittance. According to simulation results, the VT and VR curves overlap quite well with each other in the low voltage region, i.e., low to middle gray levels, but somewhat deviate in the high voltage region. Although imperfect, this can be disregarded for two reasons: 1) most of the displayed images are at middle gray levels; the RGB primaries are at the highest gray level only when displaying high luminosity of white [13] and 2) under room light condition, T-mode dominates; meanwhile, under bright sunlight, R-mode dominates. Thus, a slight mismatch in high gray levels is still acceptable for single gamma curve driving. Therefore, simulation results demonstrate that the proposed circuit is highly promising for TR-LCD applications.

IV. Conclusion

This work presents a simplified pixel circuit design for addressing single-cell-gap 2-TFT TR-LCDs to achieve single gamma curve driving. The new circuit consists of two TFTs and only one data line, subsequently enhancing the aperture ratio. Simulation results demonstrate that the stored voltages can be well matched with the required data voltages in T-region and close to the low and middle gray levels in R-region. Thus, the proposed circuit is feasible for implementation in TR-LCD panels.

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